Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A method for increasing network transmission efficiency by increasing a data updating rate of a memory for increasing efficiency of a network interface circuit transmitting data to a network, the network interface circuit including a memory and a buffer for storing at least one packet to be transmitted to the network, the method comprising:

storing a packet data corresponding to a packet in the memory;

transmitting the packet data from the memory to the buffer for storing the packet data in the buffer before transmission to the network ~~other sections of the network interface circuit for processing the packet data~~; and

storing another packet data corresponding to another packet in the memory in response to transferring the packet data from the memory to the buffer.

2 (currently amended): The method of claim 1 wherein the packet data is completely transmitted to the buffer ~~processed by the other sections of the network interface circuit~~ before another packet data is temporarily stored in the memory.

3 (currently amended): The method of claim 1 wherein ~~when~~ a portion of the packet data is transmitted to the buffer ~~processed by the other sections of the network interface circuit~~ before the memory starts to store at least a portion of another packet data for replacing the portion of the packet data.

4 (original): The method of claim 1 wherein the operation of the memory is first-in-first-out.

5 (currently amended): The method of claim 1 wherein if the packet data is divided into a first portion and a second portion, when the first portion is transmitted to the ~~network~~ buffer and the second portion is not transmitted to the ~~network~~ buffer, the memory starts to store at least a portion of another packet data.

6 (currently amended): The method of claim 5 wherein the portion of ~~when the memory starts to store at least a portion of~~ another packet data ~~, the first portion of the packet data is overwritten~~ replaces the first portion of the packet data in the memory ~~by another packet data~~.

7 (currently amended): The method of claim 5 wherein ~~the memory sequentially stores~~ the portion of another packet is sequentially stored in the memory ~~data for replacing the first portion of the packet data~~.

8-10 (cancelled)

11 (currently amended): The method of ~~claim 10~~ claim 1 wherein the operation of the buffer is first-in-first-out.

12 (cancelled)

13 (currently amended): A network interface circuit for controlling data access of a network, the network interface circuit comprising:

a medium control module for transmitting a packet to the network, the medium control module comprising a buffer for storing the packet before transmission to the network;

a memory for temporarily storing a packet data corresponding to the packet before transmitting the packet data to the buffer, the

memory including a check circuit; wherein in response to the memory transmitting ~~after the memory transmits~~ the packet data to the buffer ~~the medium control module~~, the check circuit enables the memory to generate an interrupt request signal; and

a memory access circuit; wherein after receiving the interrupt request signal, the memory access circuit stores another packet data corresponding to another packet in the memory.

14 (currently amended): The network interface circuit of claim 13 wherein after the packet data is completely transmitted to the buffer ~~processed by the other sections of the network interface circuit~~, the check circuit sends the interrupt request signal.

15 (currently amended): The network interface circuit of claim 13 wherein when a portion of the packet is transmitted to the buffer ~~processed by the other sections of the network interface circuit~~, the check circuit sends the interrupt request signal for inputting a portion of another packet.

16 (cancelled)

17 (original): The network interface circuit of claim 13 wherein the operation of the memory is first-in-first-out.

18 (currently amended): The network interface circuit of ~~claim 16~~ claim 13 wherein the operation of the buffer is first-in-first-out.

19 (original): The network interface circuit of claim 13 wherein the

network interface circuit is a full duplex network interface circuit.

20 (original): The network interface circuit of claim 13 wherein the memory controls all other memory units under a recycling memory unit operation.